Fig.1

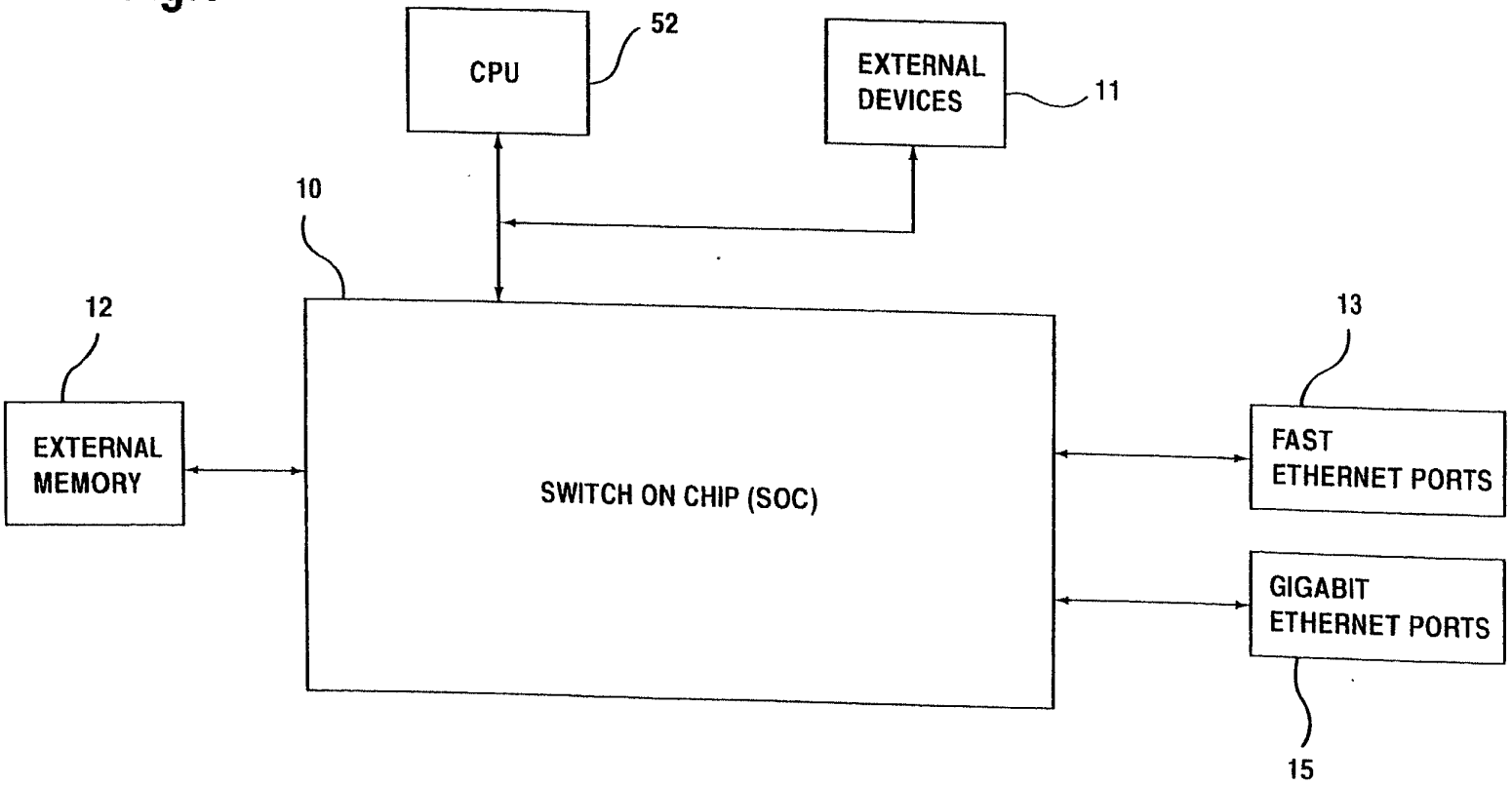

CPU
52
EXTERNAL DEVICES
11
10
12
13
EXTERNAL MEMORY
SWITCH ON CHIP (SOC)
FAST ETHERNET PORTS
GIGABIT ETHERNET PORTS
15

Fig.2

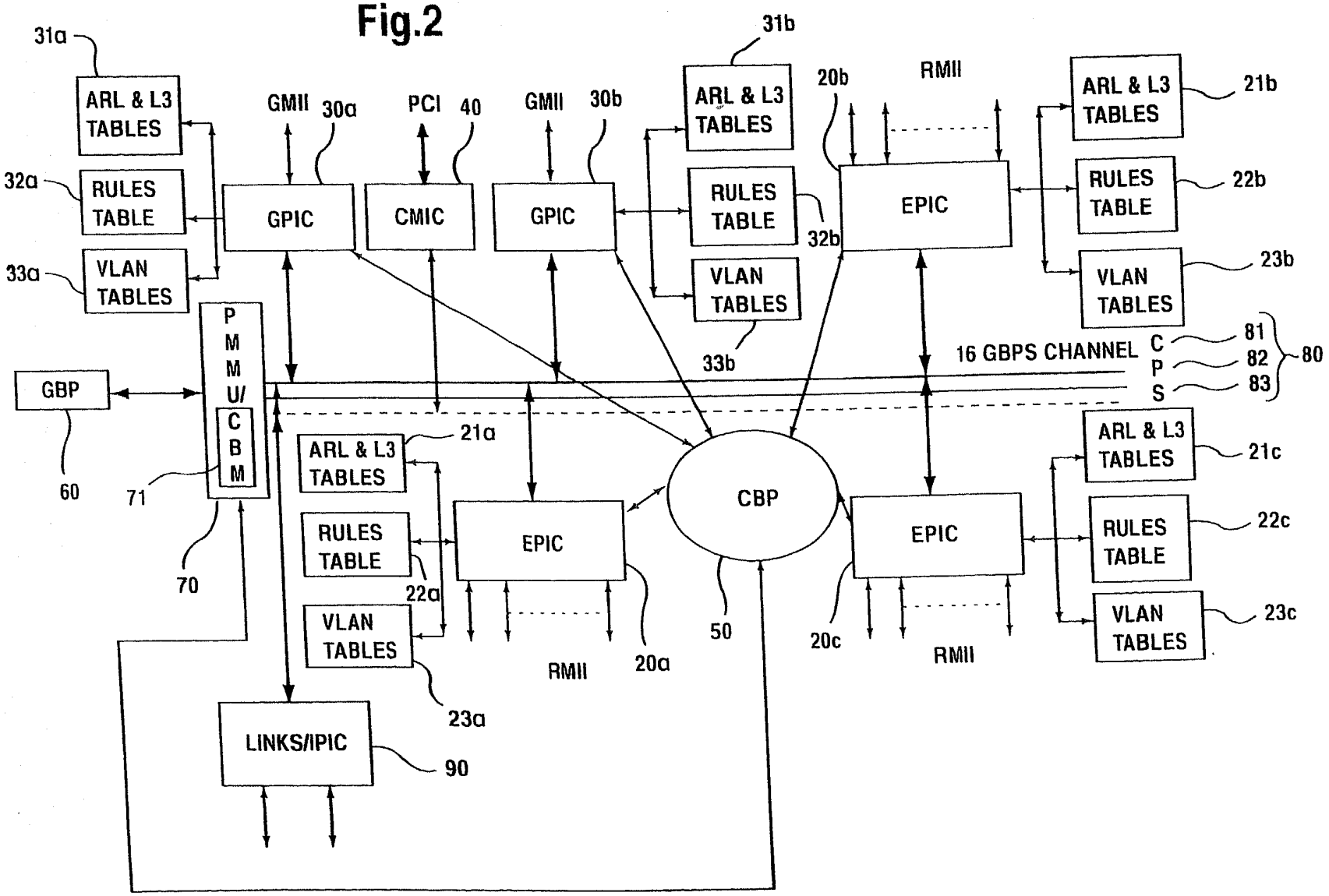

31a
ARL & L3 TABLES
32a
RULES TABLE
33a
VLAN TABLES
GMII
30a
PCI
40
GMII
30b
GPIC
CMIC
GPIC
31b
ARL & L3 TABLES
RULES TABLE
32b
VLAN TABLES
33b
20b
RMII
EPIC
ARL & L3 TABLES
21b
RULES TABLE
22b
VLAN TABLES
23b
16 GBPS CHANNEL
C
P
S
81
82
83
80
GBP
60
PMMU/CBM
71
70
ARL & L3 TABLES
21a
RULES TABLE
22a
VLAN TABLES
23a
EPIC
RMII
20a
CBP
50
EPIC
20c
RMII
ARL & L3 TABLES
21c
RULES TABLE
22c
VLAN TABLES
23c
LINKS/IPIC
90

Fig.3

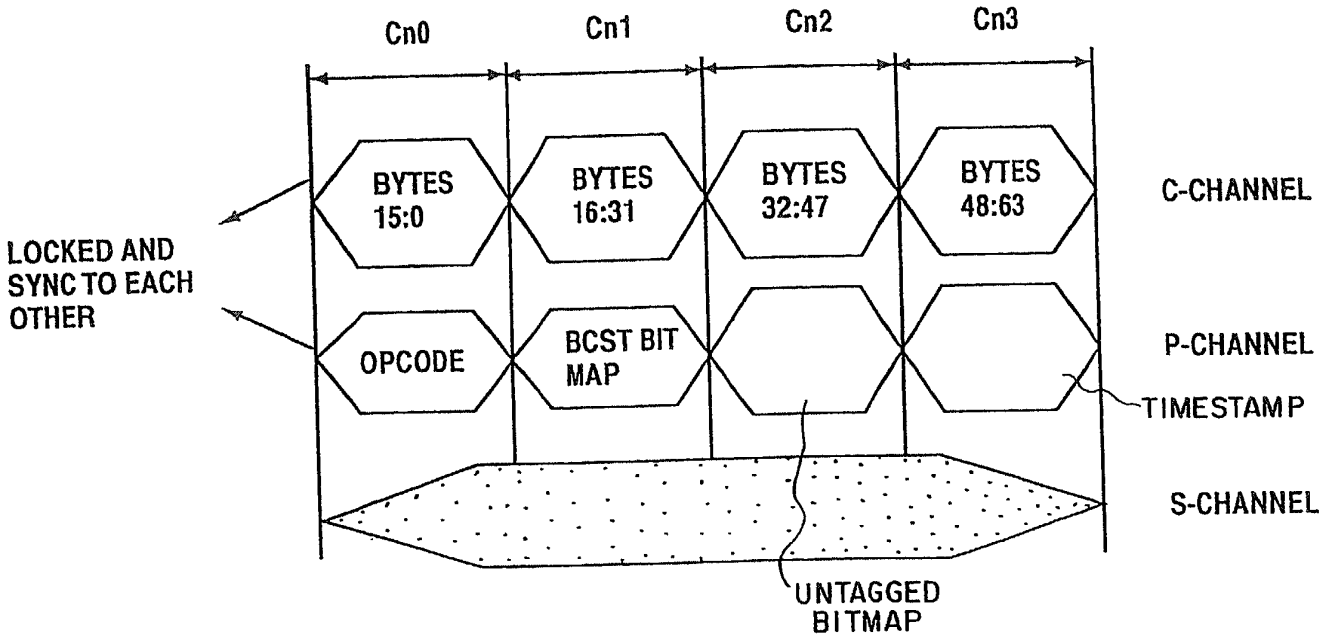

Cn0
Cn1
Cn2
Cn3
BYTES 15:0
BYTES 16:31
BYTES 32:47
BYTES 48:63
C-CHANNEL
LOCKED AND SYNC TO EACH OTHER
OPCODE
BCST BIT MAP
P-CHANNEL
TIMESTAMP
S-CHANNEL
UNTAGGED BITMAP

Fig. 4

PROTOCOL CHANNEL MESSAGES

30	28		26	24	22	20	18	16	14	12			10	8		6	4	2	0
OP CODE	I P	I P X	RESERVED	NXT CELL	SRC DEST PORT			COS		J	S	E	CR C	P	O	LEN			

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
RESERVED		BC/MC PORTBITMAP													

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
U	RES	UNTAGGED PORTBITMAP/SRC PORT NUMBER (BIT0..5)													

30	28	26	24	22	20	18	16	14	12	10	8	6	4	2	0
CPU OPCODES									TIME STAMP						

Fig. 5

SIDE BAND CHANNEL MESSAGES

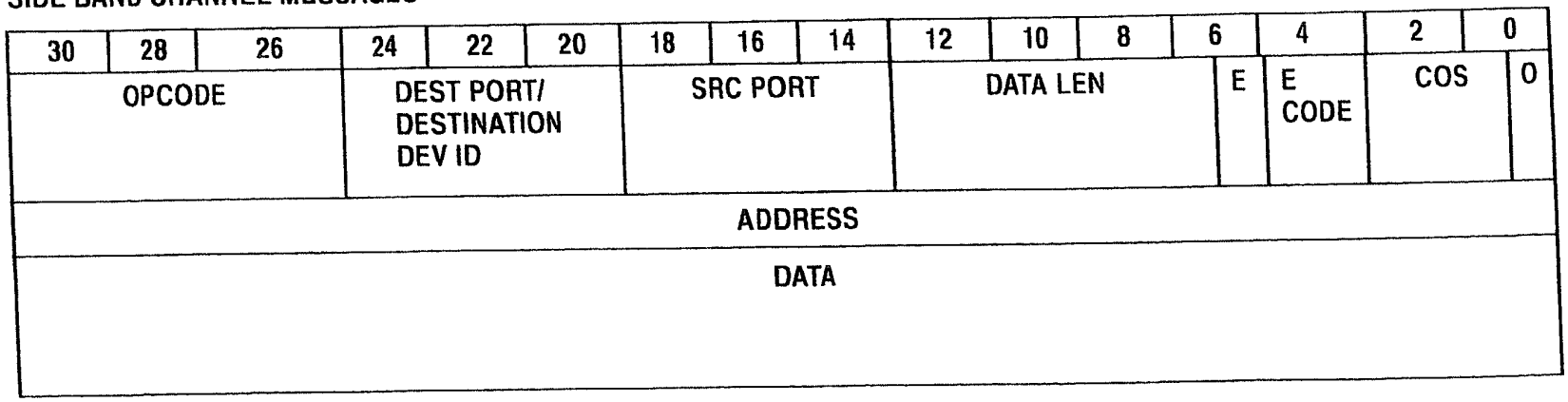


Fig. 6

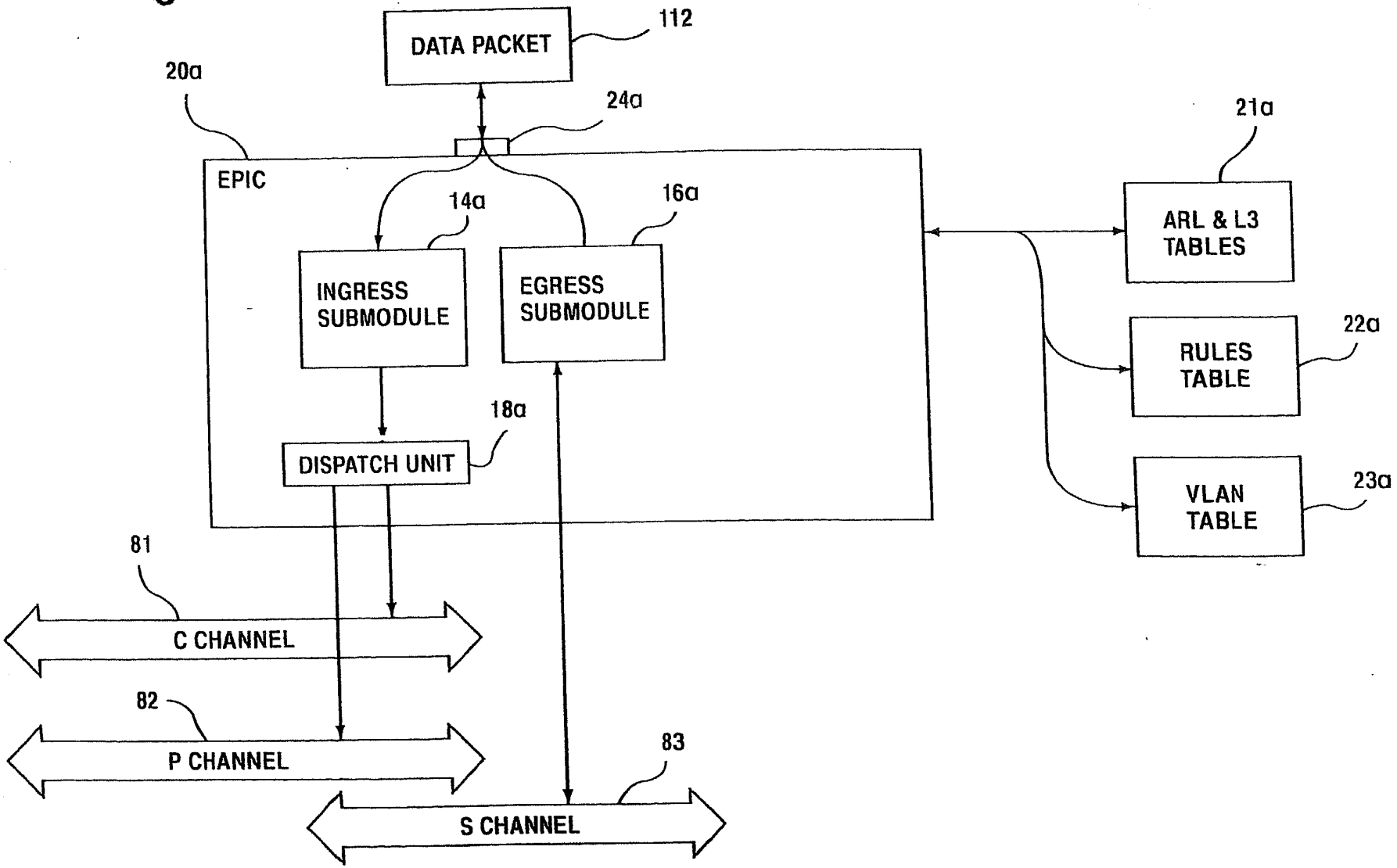

DATA PACKET
112
20a
24a
21a
EPIC
14a
16a
ARL & L3 TABLES
INGRESS SUBMODULE
EGRESS SUBMODULE
RULES TABLE
22a
18a
DISPATCH UNIT
VLAN TABLE
23a
81
C CHANNEL
82
P CHANNEL
83
S CHANNEL

Fig. 7

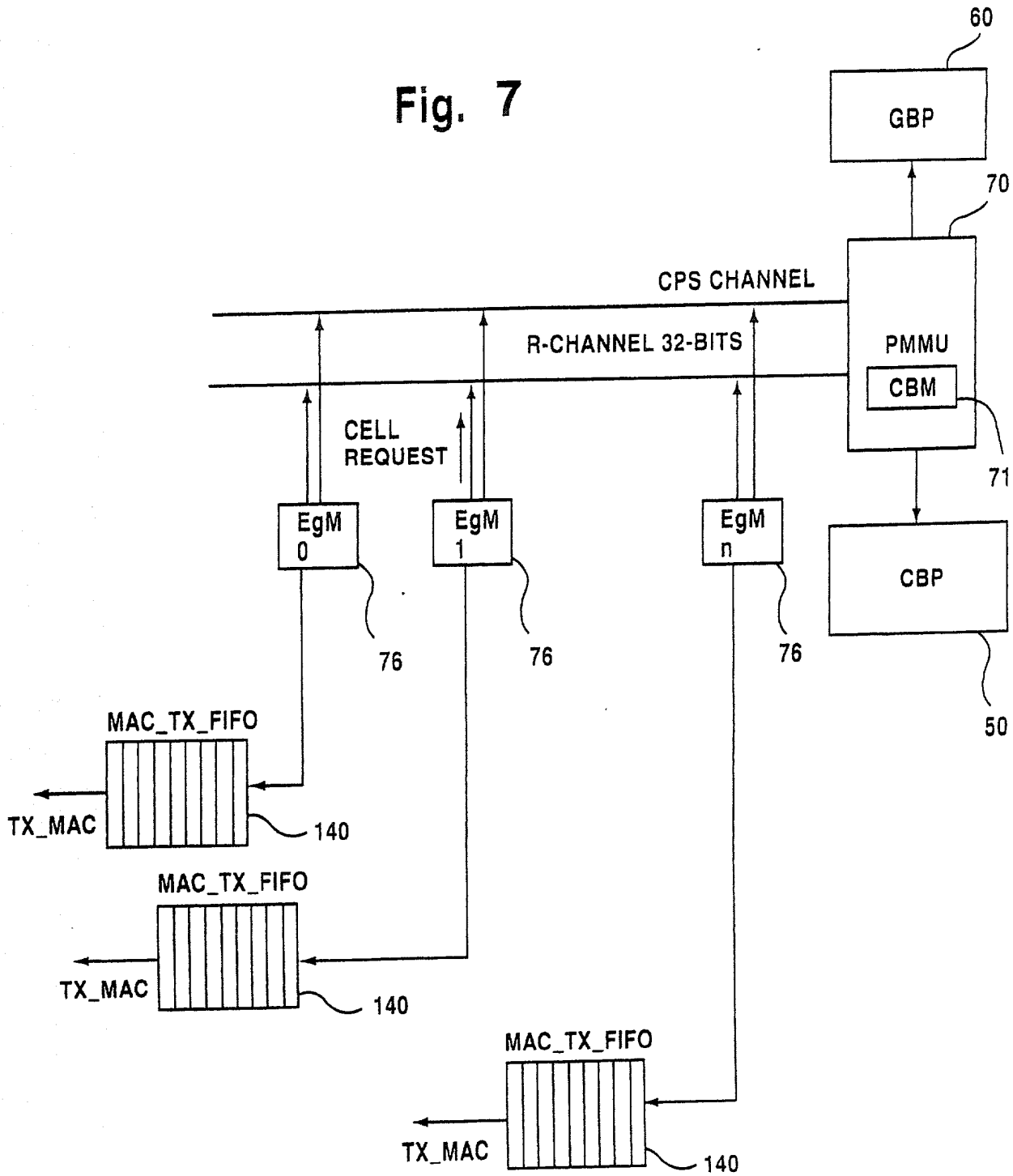
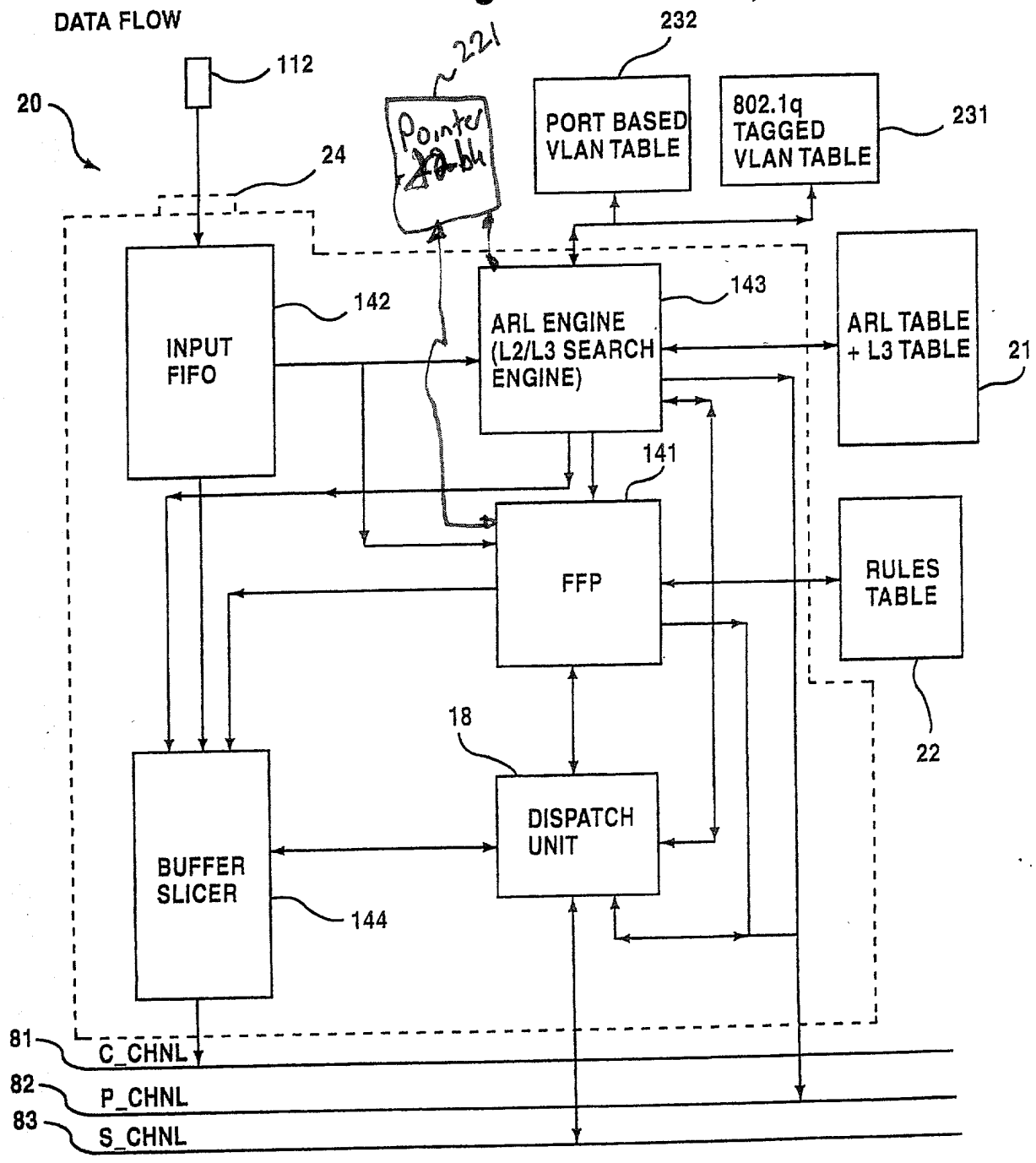

60
GBP
70
CPS CHANNEL
R-CHANNEL 32-BITS
PMMU
CBM
71
CELL
REQUEST
EgM
0
EgM
1
EgM
n
76
76
76
CBP
50
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140
MAC_TX_FIFO
TX_MAC
140

Fig. 8


DATA FLOW
112
20
24
221
Pointer
232
PORT BASED VLAN TABLE
802.1q TAGGED VLAN TABLE
231
INPUT FIFO
142
ARL ENGINE (L2/L3 SEARCH ENGINE)
143
ARL TABLE + L3 TABLE
21
141
FFP
RULES TABLE
22
18
DISPATCH UNIT
BUFFER SLICER
144
81
C_CHNL
82
P_CHNL
83
S_CHNL

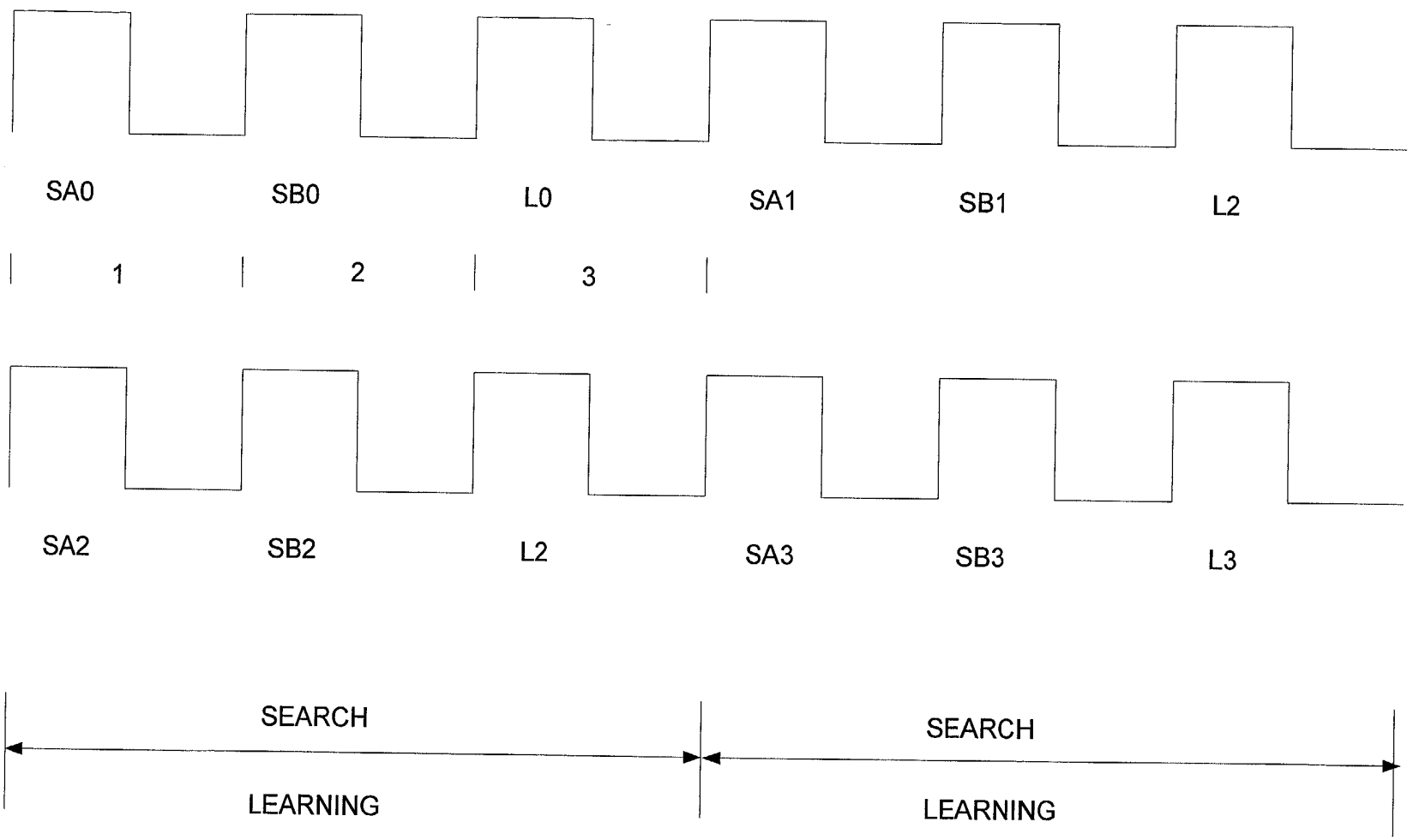

SA0
SB0
L0
SA1
SB1
L2
1
2
3
SA2
SB2
L2
SA3
SB3
L3
SEARCH
LEARNING
SEARCH
LEARNING

FIG 9

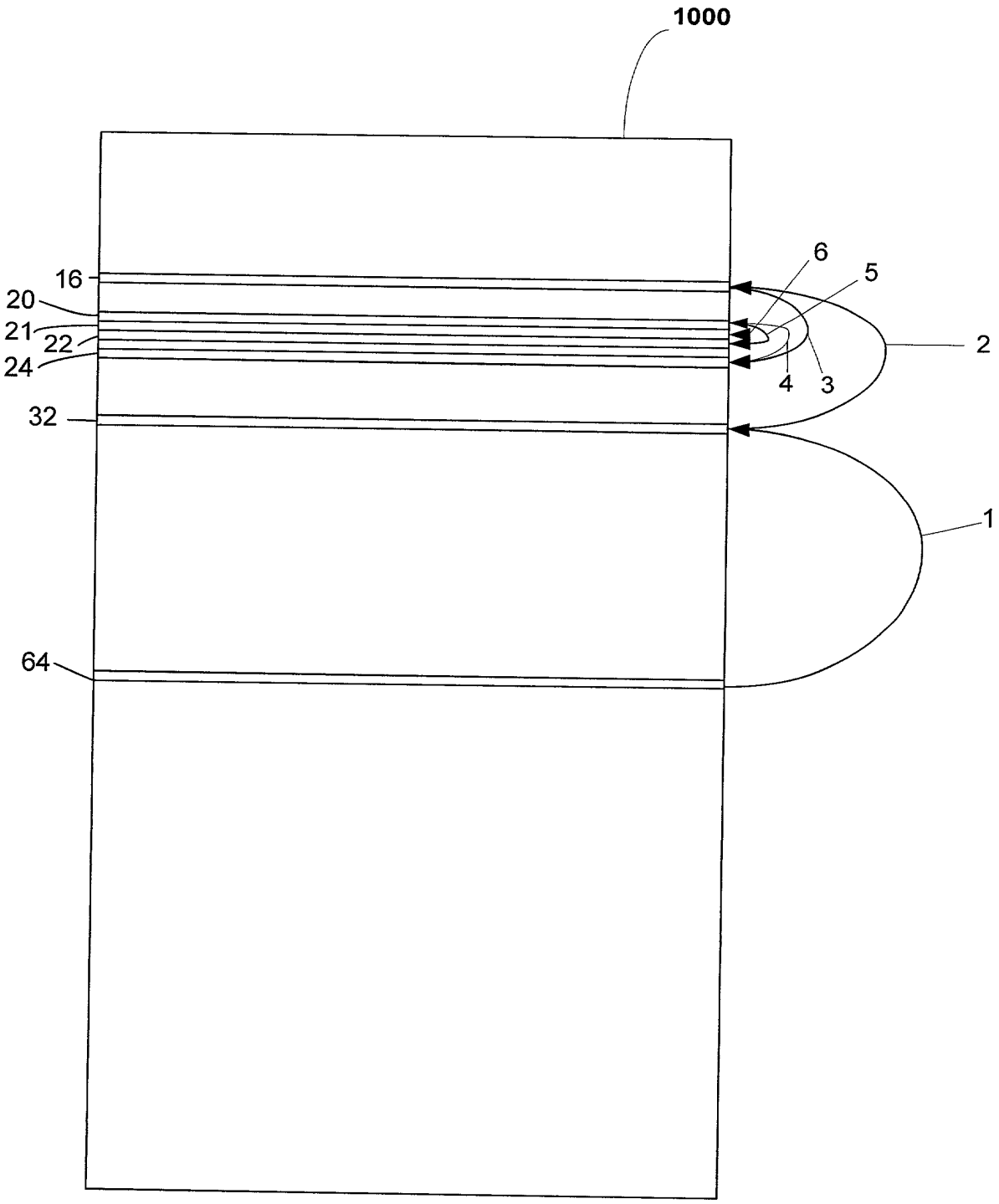


Figure 10

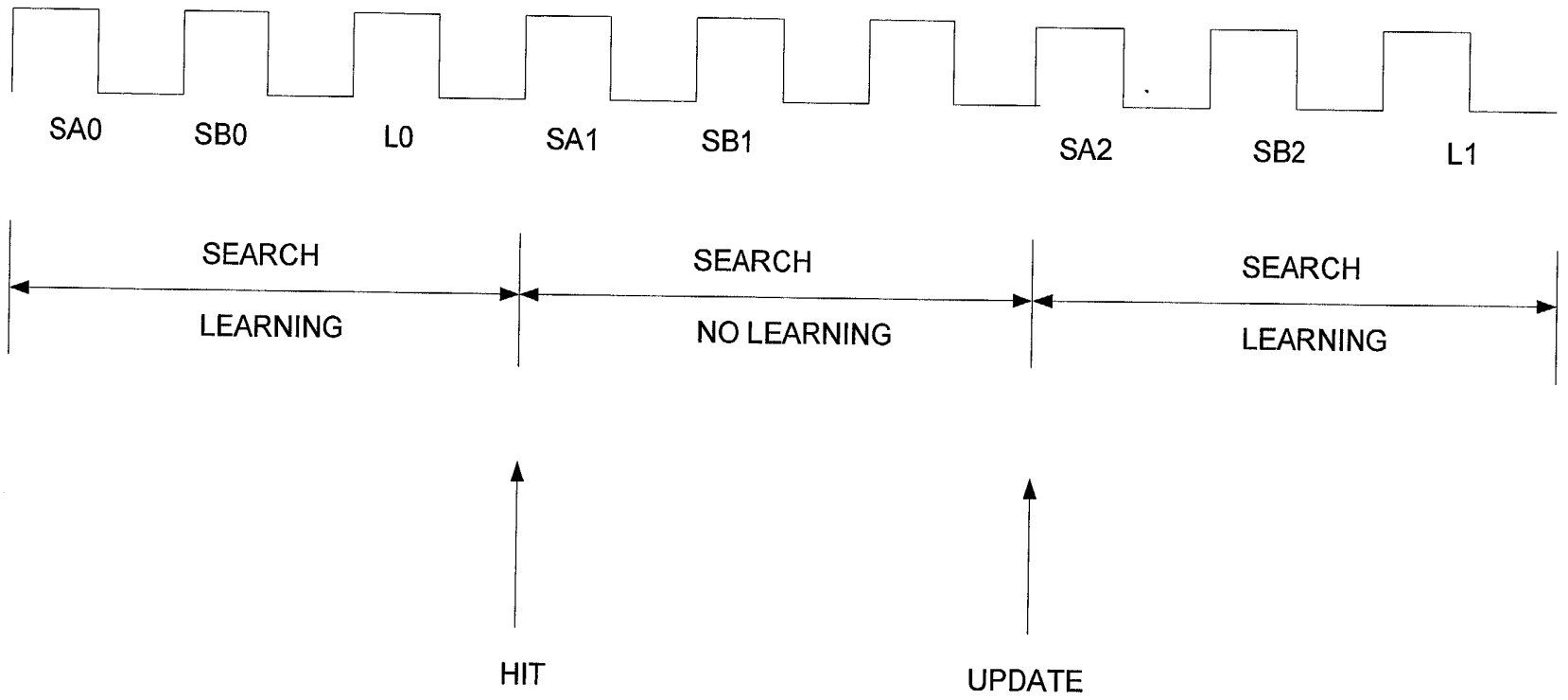

SA0
SB0
L0
SA1
SB1
SA2
SB2
L1
SEARCH
LEARNING
SEARCH
NO LEARNING
SEARCH
LEARNING
HIT
UPDATE

FIG 11

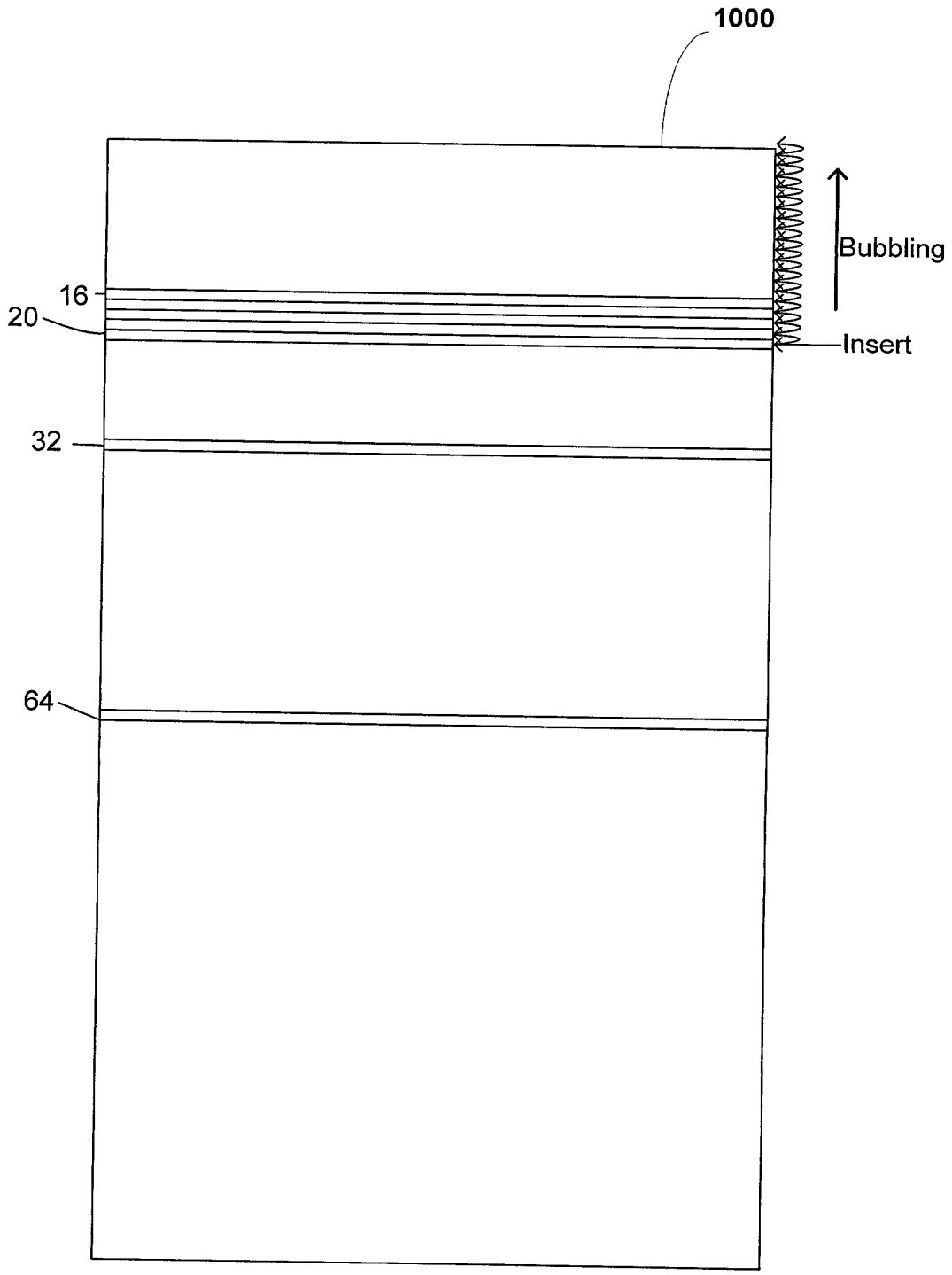


Figure 12

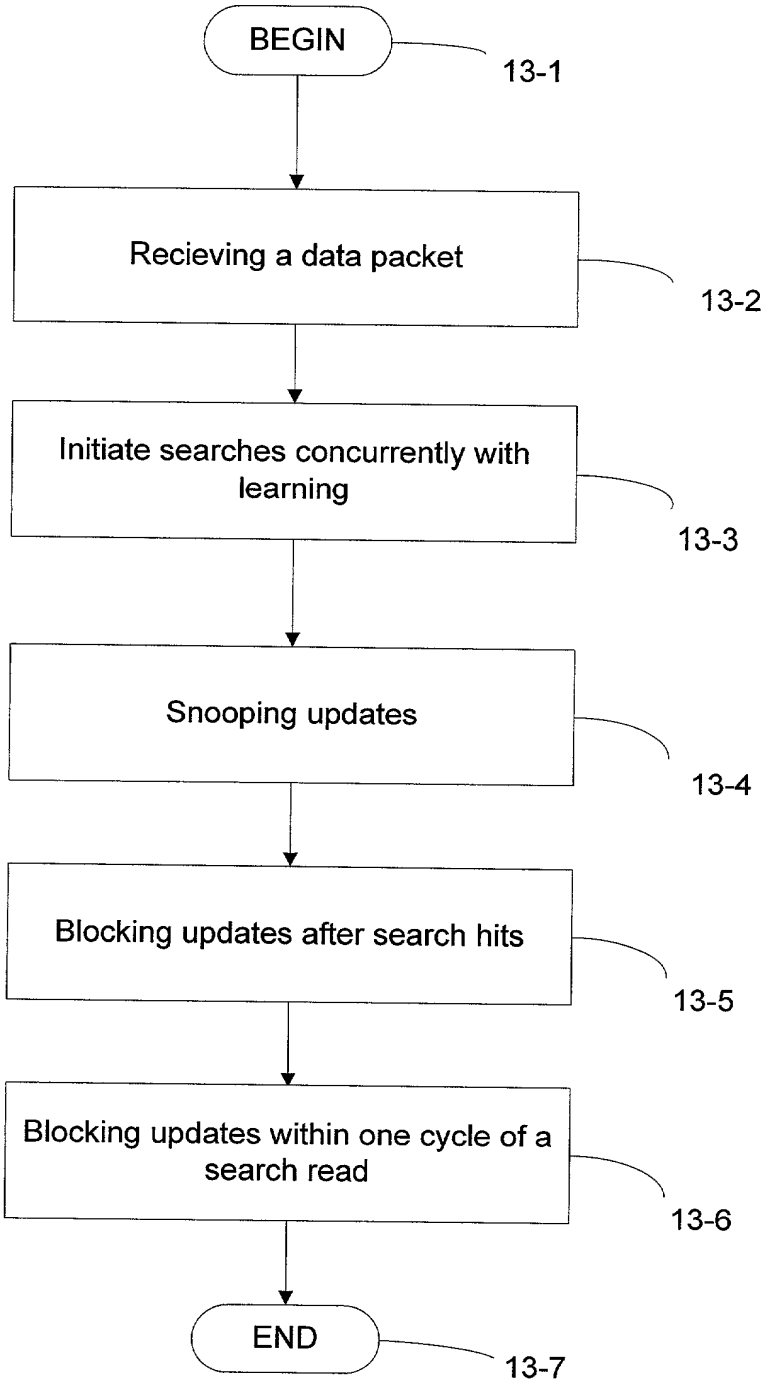

BEGIN
13-1
Recieving a data packet
13-2
Initiate searches concurrently with learning
13-3
Snooping updates
13-4
Blocking updates after search hits
13-5
Blocking updates within one cycle of a search read
13-6
END
13-7

FIG. 13